What is claimed is:

1. A method of wafer level testing, comprising:

disposing a wafer onto a chuck such that a first major surface of the wafer is adjacent the chuck;

disposing an anisotropic conductor onto a second major surface of the wafer, the second major surface of the wafer having a plurality of integrated circuits formed thereon, each of the integrated circuits having a plurality of pads;

disposing a first major surface of a translator plate onto the anisotropic conductor, such that an electrical pathway is established between at least one of the plurality of pads of each of at least two of the plurality of integrated circuits, and corresponding electrical contact pads on a second major surface of the translator plate;

engaging a clamping ring with the chuck and the translator plate;

electrically coupling the corresponding electrical contact pads to a first tester; and

applying electrical signals from the first tester to the at least two integrated circuits;

wherein applying electrical signal comprises providing power.

2. The method of Claim 1, wherein the at least two integrated circuits each have a pad layout that is the same.

3. The method of Claim 1, wherein the anisotropic conductor compensates

2 for non-planarities of the wafer and the translator plate.

1 4. The method of Claim 1, wherein the anisotropic conductor is
2 compressible.

1 5. The method of Claim 3, wherein the chuck and the translator plate each
2 include at least one clamping tab.

1 6. The method of Claim 5 wherein the at least one clamping tab of the chuck
2 has an upper surface and a lower surface and the lower surface is an inclined
3 surface.

1 7. The method of Claim 6 the at least one clamping tab of the translator plate
2 has an upper surface and a lower surface and the upper surface is an inclined
3 surface.

1 8. The method of Claim 7, wherein the clamping ring has an inner surface
2 adapted to receive the at least one clamping tab of the chuck and the at least
3 one clamping tab of the translator plate.

1 9. The method of Claim 8, wherein the inner surface of the clamping ring
2 includes an upper portion adapted to make planar contact with the inclined
3 surface of the at least one clamping tab of the translator plate, and further

includes a lower portion adapted to make planar contact with the inclined surface of the at least one clamping tab of the chuck.

10. The method of Claim 1, wherein the chuck has isolation grooves formed in the surface thereof.

11. The method of Claim 10, wherein the isolation grooves reduce thermal conduction between adjacent ones of the plurality of integrated circuits.

12. The method of Claim 11, further comprising heating one or more of the plurality of integrated circuits.

13. A method of wafer level testing, comprising:

disposing a wafer onto a first surface of a chuck such that a first surface of the wafer is adjacent the first surface of the chuck, the first surface of the chuck having isolation grooves therein;

disposing a first surface of a translator plate over a second surface of the wafer, the second surface of the wafer having a plurality of integrated circuits formed thereon, each of the integrated circuits having a plurality of pads, such that an electrical pathway is established between at least one of the plurality of pads of each of at least two of the plurality of integrated circuits, and corresponding electrical contact pads on a second surface of the translator plate;

electrically coupling the corresponding electrical contact pads to a first tester; and

applying electrical signals from the first tester to the at least two integrated circuits;

wherein the isolation grooves reduce the thermal conduction between adjacent ones of the plurality of integrated circuits.

14. The method of Claim 13, further comprising providing substantially horizontally oriented mechanical vibration to an anisotropic conductor while disposing the anisotropic conductor over the wafer.

15. The method of Claim 14, wherein providing substantially horizontally oriented mechanical vibration comprises operating a piezo-electric vibratory mechanism.

16. An apparatus, comprising:

a chuck having a first surface with isolation grooves therein, the first surface of the chuck adapted to receive a wafer thereon;

a translator plate comprising a substrate having a plurality of electrical contacts on a first surface, a corresponding plurality of electrical contacts on a second opposing surface, and a plurality of electrically conductive pathways therethrough to provide electrical continuity between the plurality of electrical

contacts on the first surface and the corresponding plurality of electrical contacts on the second opposing surface; and

a clamping ring engaged with the chuck and the translator plate such that the chuck and translator plate are held in a fixed spatial relationship with each other.

17. The apparatus of Claim 16, wherein the chuck includes at least two clamping tabs, the translator plate includes at least two clamping tabs, and wherein the clamping ring is engaged with the at least two clamping tabs of the chuck and with the at least two clamping tabs of the translator plate; and further comprising a sealing ring disposed around at least a portion of the clamping ring.

18. The apparatus of Claim 17, wherein the plurality of electrical contacts on the first surface of the translator plate have a first layout and the corresponding plurality of electrical contacts on the second opposing surface of the translator plate have a second layout, and the first layout and the second layout are different from each other.

19. A method of forming a portable assembly including a wafer, the assembly suitable for repeated testing of the wafer while preserving the integrity of the bonding pads, the method comprising:

disposing a wafer onto a chuck such that a first surface of the wafer is adjacent the chuck, the chuck having isolation grooves therein;

disposing an anisotropic conductor onto a second surface of the wafer, the second surface of the wafer having a plurality of integrated circuits formed thereon, each of the integrated circuits having a plurality of pads;

disposing a first surface of a translator plate onto the anisotropic conductor, such that an electrical pathway is established between at least one of the plurality of pads of each of at least two of the plurality of integrated circuits, and corresponding electrical contact pads on a second surface of the translator plate;

engaging a clamping ring with the chuck and the translator plate;

electrically coupling the corresponding electrical contact pads to a first tester; and

performing at least one electrical test on at least one of the plurality of integrated circuits.

20. The method of Claim 19, further comprising electrically decoupling the corresponding electrical contact pads from the first tester; moving the portable assembly; electrically coupling the corresponding electrical contact pads to a the second tester; and performing at least one electrical test on at least one of the plurality of integrated circuits.